Amendments to the Claims:

1. (Allowed) A delay equalizer for balancing clock signals in a clock tree, comprising:

a register operable to:

receive a divided input clock signal;

receive a non-divided input clock signal; and

generate a first output clock signal based on the received divided input clock signal and the received non-divided input clock signal, the first output clock signal being associated with a first delay;

a delay line operable to:

receive the non-divided input clock signal;

delay the non-divided input clock signal for a time substantially equivalent to the first delay associated with the first output clock signal; and

generate a second output clock signal being associated with a second delay substantially equal to the first delay of the first output clock signal; and

a multiplexer operable to:

receive the first output clock signal and the second output clock signal;

receive a select control signal indicating which of the first output clock signal or the second output clock signal to select, wherein the select control signal is programmable on the fly, and wherein the select control signal transitions only when the first output clock signal and the second output clock signal have the same phase;

select either the received first output clock signal or the second output clock signal based on the select control signal; and

generate the selected first output clock signal or second output clock signal as a substantially balanced third output clock signal.

2. (Currently Amended) The delay equalizer of claim 1, wherein:

the divided input clock ~~in~~ signal being associated with a functional mode of a device comprising the delay equalizer; and

the select control signal received by the multiplexer comprises a divided/non-divided select control signal;

the delay equalizer is operable to substantially balance an ~~the~~ input clock signal between one or more functional modes of the device.

3. (Allowed) The delay equalizer of claim 2, wherein the delay equalizer is implemented at the output of existing clock dividing and selection logic.

4. (Allowed) The delay equalizer of claim 2, wherein the delay equalizer is implemented within existing clock dividing and selection logic, the clock dividing and selection logic being redesigned to include the delay equalizer.

5. (Allowed) The delay equalizer of claim 1, wherein the delay equalizer is associated with a clock-gating cell and is operable to provide the substantially balanced third output clock signal to the clock-gating cell as an input clock signal to the clock-gating cell such that an output clock signal generated by the clock-gating cell is substantially balanced.

6. (Allowed) The delay equalizer of claim 1, wherein:

the register comprises a flip-flop register; and

the delay line comprises one or more buffers for delaying the non-divided clock signal.

7. (Allowed) A method for balancing clock signals in a node of a clock tree, comprising:

receiving a divided input clock signal at a register;

receiving a non-divided input clock signal at the register;

generating at the register a first output clock signal based on the received divided input clock signal and the received non-divided input clock signal, the first output clock signal being associated with a first delay; receiving the non-divided input clock signal at a delay line;

delaying at the delay line the non-divided input clock signal for a time substantially equivalent to the first delay associated with the first output clock signal;

generating at the delay line a second output clock signal being associated with a second delay substantially equal to the first delay of the first output signal;

receiving at a multiplexer the first output clock signal and the second output clock signal;

receiving at the multiplexer a select control signal indicating which of the first output clock signal or the second output clock signal to select, wherein the select control signal is programmable on the fly, and wherein the select control signal transitions only when the first output clock signal and the second output clock signal have the same phase;

selecting at the multiplexer either the received first output clock signal or the second output clock signal based on the select control signal; and

generating the selected first output clock signal or second output clock signal as a substantially balanced third output clock signal.

8. (Currently Amended) The method of claim 7, wherein:

the divided input clock ~~in~~ signal being associated with a functional mode of a device comprising the delay equalizer; and

the select control signal received by the multiplexer comprises a divided/non-divided select control signal;

the method substantially balancing an ~~the~~ input clock signal between one or more functional modes of the device.

9. (Allowed) The method of claim 8, wherein the method is performed on the output of existing clock dividing and selection logic.

10. (Allowed) The method of claim 8, wherein the method is integrated into existing clock dividing and selection logic, the clock dividing and selection logic having been redesigned for implementing the method.

11. (Allowed) The method of claim 7, further comprising providing the substantially balanced third output clock signal to a clock-gating cell as an input clock signal to the clock-gating cell such that an output clock signal generated by the clock-gating cell is substantially balanced.

12. (Allowed) The method of claim 7, wherein:
the register comprises a flip-flop register; and
the delay line comprises one or more buffers for delaying the non-divided clock signal.

13. (Canceled).

14. (Canceled).

15. (Canceled).

16. (Canceled).

17. (Canceled).

18. (Canceled).

19. (Canceled).

20. (Canceled).

21. (Currently Amended) The method of claim 7 ~~1~~, wherein the select control signal transitions substantially coincident with a rising edge of the first output clock signal and a rising edge of the second output clock signal in the same phase.

22. (Currently Amended) The method of claim 7 ~~1~~, wherein the multiplexer is further operable to:

isolate the first output clock signal and the second output clock signal from a clock load.

23. (Canceled).

24. (New) The delay equalizer of claim 1, wherein the select control signal transitions substantially coincident with a rising edge of the first output clock signal and a rising edge of the second output clock signal in the same phase.

25. (New) The delay equalizer of claim 1, wherein the multiplexer is further operable to:

isolate the first output clock signal and the second output clock signal from a clock load.